What Is Claimed Is:

1. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions, the active regions each comprising a first layer of insulation material on the semiconductor substrate and a first layer of conductive material on the first layer of insulation material;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction, each of the first trenches having an upper portion and a lower portion wherein the upper portion has a greater width than that of the lower portion;

c) filling each of the first trenches with a conductive material to form first blocks of conductive material, wherein for each of the first blocks in each active region:

the first block includes a lower portion formed in the lower portion of the first trench that is disposed adjacent to and insulated from the first layer of conductive material, and

the first block includes an upper portion formed in the upper portion of the first trench that is disposed over and insulated from the first layer of conductive material;

d) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals is adjacent to and electrically connected with one of the first blocks of conductive material; and

e) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals.

2. The method of claim 1, wherein the first blocks of conductive material are substantially T-shaped.

3. The method of claim 1, further comprising the step of:

forming a layer of metalized silicon on each of the first blocks of conductive material.

4. The method of claim 1, further comprising the step of:

forming a second layer of conductive material in the first trenches before forming the first blocks of conductive material.

5. The method of claim 1, further comprising the step of:

forming a second layer of insulation material along sidewalls of each of the first trenches, wherein the lower and upper portions of each of the first blocks are insulated from the first layer of conductive material by the second layer of insulation material.

6. The method of claim 1, further comprising the step of:

forming a plurality of spaced apart second trenches which are substantially parallel to one another and to the first trenches;

forming second blocks of a conductive material in the second trenches, wherein for each of the second blocks of conductive material:

the second block includes a lower portion that is disposed adjacent to and insulated from the first layer of conductive material, and

the second block includes an upper portion that is disposed over and insulated from the first layer of conductive material.

7. The method of claim 6, further comprising the step of:

forming a layer of metalized silicon on each of the second blocks of conductive material.

8. The method of claim 1, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of a first material over the first layer of conductive material,

selectively etching through the at least one layer of first material to form the top portions of the first trenches;

forming at least one layer of a second material along a bottom surface of the first trenches;

forming side wall spacers on side walls of each of the first trenches;

etching between the side wall spacers in each of the first trenches and through the at least one layer of second material to expose portions of the first layer of conductive material; and

etching the exposed portions of the first layer of conductive material to form the bottom portions of the first trenches;

wherein the bottom portions of the first trenches have a smaller width than that of the top portions of the first trenches.

9. The method of claim 6, further comprising the steps of:

forming a side wall spacer of insulating material along a side wall of each of the second blocks of conductive material; and

forming a layer of metalized silicon on each of the second terminals, wherein each of the layers of metalized silicon is self-aligned to the one of the side wall spacers.

10. The method of claim 9, further comprising the step of:

forming a conductive material over each of the layers of metalized silicon and against the side wall spacer self aligned thereto.

11. The method of claim 9, wherein the formation of each of the side wall spacers includes forming a layer of insulation material between the side wall spacer and the side wall of the second block of conductive material.

12. The method of claim 6, further comprising the steps of:

forming third blocks of a material in the second trenches and adjacent to the second blocks of conductive material;

forming a layer of metalized silicon on each of the second blocks of conductive material, wherein for each of the second trenches, a side wall of one of the third blocks of material aligns an edge of the metalized silicon layer to an edge of the second block of conductive material; and

forming a second layer of insulation material over the layer of metalized silicon, wherein for each of the second trenches, the side wall of the one third block of material aligns an edge of the second layer of insulation material to the edge of the metalized silicon and to the edge of the second block of conductive material.

13. The method of claim 6, further comprising the steps of:

forming a side wall spacer of insulating material along a side wall of each of the second blocks of conductive material such that pairs of the side wall spacers are adjacent to but spaced apart from each other with one of the second terminals substantially therebetween;

forming a layer of metalized silicon on each one of the second terminals between a pair of the side wall spacers corresponding to the one second terminal such that the layer of metalized silicon is self-aligned to the one second terminal by the corresponding pair of side wall spacers;

forming a layer of protective insulation material over the second blocks of conductive material;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of side wall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of side wall spacers; and

filling each of the contact openings with a conductive material.

14. A self-aligned method of forming a semiconductor memory array of floating gate memory cells in a semiconductor substrate, each memory cell having a floating gate, a first terminal, a second terminal with a channel region therebetween, and a control gate, the method comprising the steps of:

a) forming a plurality of spaced apart isolation regions on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between

each pair of adjacent isolation regions, the active regions each comprising a first layer of insulation material on the semiconductor substrate and a first layer of conductive material on the first layer of insulation material;

b) forming a plurality of spaced apart first trenches across the active regions and isolation regions which are substantially parallel to one another and extend in a second direction that is substantially perpendicular to the first direction, each of the first trenches having a side wall with an indentation formed therein;

c) filling each of the first trenches with a conductive material to form first blocks of conductive material, wherein for each of the first blocks in each active region:

the first block includes a lower portion formed below the indentation of the first trench sidewall that is disposed adjacent to and insulated from the first layer of conductive material, and

the first block includes an upper portion formed above the indentation of the first trench sidewall that is disposed over and insulated from the first layer of conductive material;

d) forming a plurality of first terminals in the substrate, wherein in each of the active regions each of the first terminals is adjacent to and electrically connected with one of the first blocks of conductive material; and

e) forming a plurality of second terminals in the substrate, wherein in each of the active regions each of the second terminals is spaced apart from the first terminals.

15. The method of claim 14, wherein the first blocks of conductive material are substantially T-shaped.

16. The method of claim 14, further comprising the step of:
forming a layer of metalized silicon on each of the first blocks of conductive material.

17. The method of claim 14, further comprising the step of:
forming a second layer of conductive material in the first trenches before forming the first blocks of conductive material.

18. The method of claim 14, further comprising the step of:

forming a second layer of insulation material along sidewalls of each of the first trenches, wherein the lower and upper portions of each of the first blocks are insulated from the first layer of conductive material by the second layer of insulation material.

19. The method of claim 14, further comprising the step of:

forming a plurality of spaced apart second trenches which are substantially parallel to one another and to the first trenches;

forming second blocks of a conductive material in the second trenches, wherein for each of the second blocks of conductive material:

the second block includes a lower portion that is disposed adjacent to and insulated from the first layer of conductive material, and

the second block includes an upper portion that is disposed over and insulated from the first layer of conductive material.

20. The method of claim 19, further comprising the step of:

forming a layer of metalized silicon on each of the second blocks of conductive material.

21. The method of claim 14, wherein the formation of the first trenches comprises the steps of:

forming at least one layer of a first material over the first layer of conductive material,

selectively etching through the at least one layer of first material to form the top portions of the first trenches;

forming at least one layer of a second material along a bottom surface of the first trenches;

forming side wall spacers on side walls of each of the first trenches;

etching between the side wall spacers in each of the first trenches and through the at least one layer of second material to expose portions of the first layer of conductive material; and

etching the exposed portions of the first layer of conductive material to form the bottom portions of the first trenches;

wherein the sidewall indentations are formed between the top and bottom portions of the first trenches.

22. The method of claim 19, further comprising the steps of:

forming a side wall spacer of insulating material along a side wall of each of the second blocks of conductive material; and

forming a layer of metalized silicon on each of the second terminals, wherein each of the layers of metalized silicon is self-aligned to the one of the side wall spacers.

23. The method of claim 22, further comprising the step of:

forming a conductive material over each of the layers of metalized silicon and against the side wall spacer self aligned thereto.

24. The method of claim 22, wherein the formation of each of the side wall spacers includes forming a layer of insulation material between the side wall spacer and the side wall of the second block of conductive material.

25. The method of claim 19, further comprising the steps of:

forming third blocks of a material in the second trenches and adjacent to the second blocks of conductive material;

forming a layer of metalized silicon on each of the second blocks of conductive material, wherein for each of the second trenches, a side wall of one of the third blocks of material aligns an edge of the metalized silicon layer to an edge of the second block of conductive material; and

forming a second layer of insulation material over the layer of metalized silicon, wherein for each of the second trenches, the side wall of the one third block of material aligns an edge of the second layer of insulation material to the edge of the metalized silicon and to the edge of the second block of conductive material.

26. The method of claim 19, further comprising the steps of:

forming a side wall spacer of insulating material along a side wall of each of the second blocks of conductive material such that pairs of the side wall spacers are adjacent to but spaced apart from each other with one of the second terminals substantially therebetween;

forming a layer of metalized silicon on each one of the second terminals between a pair of the side wall spacers corresponding to the one second terminal such that the layer of metalized silicon is self-aligned to the one second terminal by the corresponding pair of side wall spacers;

forming a layer of protective insulation material over the second blocks of conductive material;

forming a layer of passivation material over the active regions;

forming contact openings through the passivation material, wherein for each of the contact openings:

the contact opening extends down to and exposes one of the metalized silicon layers,

the contact opening has a lower portion bounded by the corresponding pair of side wall spacers, and

the contact opening has an upper portion that is wider than a spacing between the corresponding pair of side wall spacers; and

filling each of the contact openings with a conductive material.

27. An electrically programmable and erasable memory device comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions in the substrate of a second conductivity type, with a channel region therebetween;

a first insulation layer disposed over said substrate;

an electrically conductive floating gate disposed over said first insulation layer and extending over a portion of said channel region and over a portion of the first region; and

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is disposed adjacent to and insulated from the floating gate and an upper portion that is disposed over and insulated from the floating gate.

28. The device of claim 27, wherein the source region upper portion has a greater width than that of the source region lower portion.

29. The device of claim 28, wherein the source region has a substantially T-shaped cross-section.

30. The device of claim 27, further comprising:

a second insulation layer disposed over and adjacent the floating gate and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed adjacent to the second insulation layer and the floating gate, and the second control gate portion being disposed over a portion of the second insulation layer and a portion of the floating gate.

31. An array of electrically programmable and erasable memory devices comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

a first insulation layer disposed over said substrate including over the channel regions,

a pair of electrically conductive floating gates each disposed over the first insulation layer and extending over a portion of one of the channel regions and over a portion of the first region, and

an electrically conductive source region disposed over and electrically connected to the first region in the substrate, the source region having a lower portion that is

disposed adjacent to and insulated from the pair of floating gates and an upper portion that is disposed over and insulated from the pair of floating gates.

32. The device of claim 31, wherein the source region upper portion has a greater width than that of the source region lower portion.

33. The device of claim 32, wherein the source region has a substantially T-shaped cross-section.

34. The device of claim 31, wherein each of the source regions extends across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions.

35. The device of claim 31, wherein each of the memory cell pairs further comprises:

a second insulation layer disposed over and adjacent to each of the floating gates and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough; and

a pair of electrically conductive control gates each having a first portion and a second portion, the first control gate portion being disposed adjacent to the second insulation layer and one of the floating gates, and the second control gate portion being disposed over a portion of the second insulation layer and a portion of the one floating gate.

36. The device of claim 35, wherein each of the control gates extends across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions.